IN THE CLAIMS

Please amend the claims as follows:

Claims 1-37 (Canceled).

Claim 38 (New): A method for assembling a first and a second wafer, of which at least the first wafer has at least a chamfered edge, the method comprising:

covering the first wafer with a protective layer;

routing at least one part of the chamfered edge of the first wafer;

eliminating the protective layer after routing the first wafer; and

then, assembling the first wafer routed and the second wafer.

Claim 39 (New): A method as in claim 38, further comprising, after the assembling, thinning out at least the first wafer, leaving at least a layer on the second wafer.

Claim 40 (New): A method as in claim 38, wherein the protective layer is eliminated locally, before routing the first wafer, in a zone located above a zone to be routed of the first wafer.

Claim 41 (New): A method as in claim 40, wherein the local elimination of the protective layer is performed via lithography and etching.

Claim 42 (New): A method as in claim 39, wherein the routing is performed over an entire thickness of the first wafer.

Claim 43 (New): A method as in claim 38, wherein the routing is performed over a thickness less than an entire thickness of the first wafer.

Claim 44 (New): A method as in claim 43, wherein the routing is performed over a thickness greater than or equal to a thickness of a layer of the first wafer to be transplanted onto the second wafer.

Claim 45 (New): A method as in claim 43, wherein the routing is performed over a thickness less than or equal to a thickness of a layer of the first wafer to be transplanted or transferred onto the second wafer.

Claim 46 (New): A method as in claim 38, wherein the routing is performed over a width, measured on a plane parallel to that of the first wafer, at least equal to a width of the chamfered edge, measured on the same plane.

Claim 47 (New): A method as in claim 38, further comprising an additional routing after assembling the first and second wafers.

Claim 48 (New): A method as in claim 38, wherein the routing is performed over a thickness of the first wafer of between 1 μm and 100 μm.

Claim 49 (New): A method as in claim 38, wherein the routing is performed over a width, measured on a plane parallel to that of the first wafer, at least equal to a width of a zone of a first wafer which can not, without routing, be assembled with the second wafer.

Claim 50 (New): A method as in claim 38, wherein the routing is performed over a width, measured on a plane parallel to that of the first wafer, of between 100 μm and 5 mm.

Claim 51 (New): A method as in claim 38, wherein the first wafer has a weakened plane defining a thin layer in the wafer.

Claim 52 (New): A method as in claim 51, wherein the first wafer is routed over a thickness greater than that of the thin layer.

Claim 53 (New): A method as in claim 52, further comprising:

thinning out via separation of the first wafer along the weakened plane, so as to leave the thin layer on the second wafer and leave a free portion of the first substrate;

creating a new weakened plane in the portion that remained free of the first substrate; and

assembling the portion with a third substrate.

Claim 54 (New): A method as in claim 51, wherein the weakened plane is formed via ion implantation or via creating a buried porous zone or via creating a removable bonding interface.

Claim 55 (New): A method as in claim 38, wherein the first wafer includes a lateral shoulder, eliminated during the routing.

Claim 56 (New): A method as in claim 38, wherein the assembling the first and second wafers is performed via molecular adhesion or via bonding using an adhesive substance.

Claim 57 (New): A method as in claim 38, wherein components or circuits are made in the first wafer before the routing.

Claim 58 (New): A method as in claim 38, wherein the routing takes place after a previous surface preparation of the first wafer for a purpose of assembling or transplanting.

Claim 59 (New): A method as in claim 38, wherein the routing takes place before a previous surface preparation of the first wafer for a purpose of assembling or transplanting.

Claim 60 (New): A method as in claim 38, wherein the routing is performed via mechanical or chemical or mechano-chemical etching or polishing or via plasma etching or via a combination of at least two of these types of etching.

Claim 61 (New): A method as in claim 38, wherein at least one of the two wafers is made in a semiconductor material.

Claim 62 (New): A method as in claim 38, wherein at least one of the two wafers is made in silicon or in a III-V type semiconductor material.

Claim 63 (New): A method as in claim 38, wherein at least one of the two wafers is made in Germanium or in Germanium silicide (SiGe) or in a piezoelectric material or in an insulating material.

Claim 64 (New): A method as in claim 38, wherein the routing is performed in a regular manner around the first wafer.

Claim 65 (New): A method as claimed in claim 38, wherein the routing is performed in an irregular manner around the first wafer, creating a plane.

Claim 66 (New): A method as in claim 38, wherein the routing is performed in an irregular manner, creating a marking zone.

Claim 67 (New): A method as in claim 66, further comprising marking the first wafer.

Claim 68 (New): A method for transplanting a transplant layer of material or circuits or components, comprising:

routing a first wafer of material, in which the transplant layer is made, at least around or on a periphery of the transplant layer, over a thickness less than a thickness of the first wafer, but greater than a thickness of the transplant layer; and

transplanting the transplant layer onto a second wafer or material.

Claim 69 (New): A method as in claim 68, wherein the first wafer previously is covered with a protective layer.

Claim 70 (New): A method as in claim 69, wherein the protective layer is eliminated locally, before routing the first waver, in a zone located above a zone to be routed of the first wafer.

Claim 71 (New): A method as in claim 70, wherein the local elimination of the protective layer is performed via lithography and etching.

Claim 72 (New): A method as in claim 69, wherein the protective layer is eliminated after routing the first wafer.

Claim 73 (New): A method as in claim 68, wherein a part of the material of the transplant layer is eliminated during the routing.

Claim 74 (New): A method as in claim 68, wherein the first wafer is chamfered and includes at least a chamfered edge.

Claim 75 (New): A method as in claim 74, wherein the routing is performed over a width, measured on a plane parallel to that of the first wafer, at least equal to a width of the chamfered edge, measured on the same plane.

Claim 76 (New): A method as in claim 68, further comprising an additional routing after assembling the first and second wafers.

Claim 77 (New): A method as in claim 68, wherein the routing is performed over a thickness of the first wafer between 1 μm and 100 μm.

Claim 78 (New): A method as in claim 68, wherein the routing is performed over a width, measured on a plane parallel to that of the first wafer, at least equal to a width of a zone of the first wafer which can not, without routing, be assembled with the second wafer.

Claim 79 (New): A method as in claim 68, wherein the routing is performed over a width, measured on a plane parallel to that of the first wafer of between 100 μm and 5 mm.

Claim 80 (New): A method as in claim 38, wherein the first wafer has a weakened plane defining a thin layer in the wafer.

Claim 81 (New): A method as in claim 80, wherein the first wafer is routed over a thickness greater than that of the thin layer.

Claim 82 (New): A method as in claim 81, further comprising:

thinning out, via separation of the first wafer along the weakened plane, so as to leave the thin layer on the second wafer and leave a free portion of the first substrate;

creating a new weakened plane in the portion that remained free of the first substrate; and

assembling the portion with a third substrate.

Claim 83 (New): A method as in claim 81, wherein the weakened plane is performed via ion implantation or via creating a buried porous zone or via creating a removable bonding interface.

Claim 84 (New): A method as in claim 38, wherein the first wafer includes a lateral shoulder, eliminated during the routing.

Claim 85 (New): A method as in claim 68, wherein the assembling the first and second wafers is performed via molecular adhesion or via bonding using an adhesive substance.

Claim 86 (New): A method as in claim 68, wherein components or circuits are made in the first wafer before the routing.

Claim 87 (New): A method as in claim 68, wherein the routing takes place after a previous surface preparation of the first wafer for a purpose of assembling or transplanting.

Claim 88 (New): A method as in claim 68, wherein the routing takes place before a previous surface penetration of the first wafer for a purpose of assembling or transplanting.

Claim 89 (New): A method as in claim 68, wherein the routing is performed via mechanical or chemical or mechano-chemical etching or polishing or via plasma etching or via a combination of at least two of these types of etching.

Claim 90 (New): A method as in claim 68, wherein at least one of the two wafers is made in a semiconductor material.

Claim 91 (New): A method as in claim 68, wherein at least one of the two wafers is made in silicon or in a III-V type semiconductor material.

Claim 92 (New): A method as in claim 68, wherein at least one of the two wafers is made in Germanium or in Germanium silicide (SiGe) or in a piezoelectric material or in an insulating material.

Claim 93 (New): A method as in claim 68, wherein the routing is performed in a regular manner around the first wafer.

Claim 94 (New): A method as in claim 68, wherein the routing is performed in an irregular manner around the first wafer, creating a plane.

Claim 95 (New): A method as in claim 68, wherein the routing is performed in an irregular manner, creating a marking zone.

Claim 96 (New): A method as in claim 95, further comprising marking the first wafer.

Claim 97 (New): A method for assembling a first and a second wafer, of which at least the first wafer has at least a chamfered edge, the method comprising:

covering the first wafer with a protective layer;

routing at least one part of the chamfered edge of the first wafer and of the protective layer, in a zone located above a zone of the first wafer to be routed;

eliminating the protective layer after routing the first wafer; and

then, assembling the first wafer routed and the second wafer.